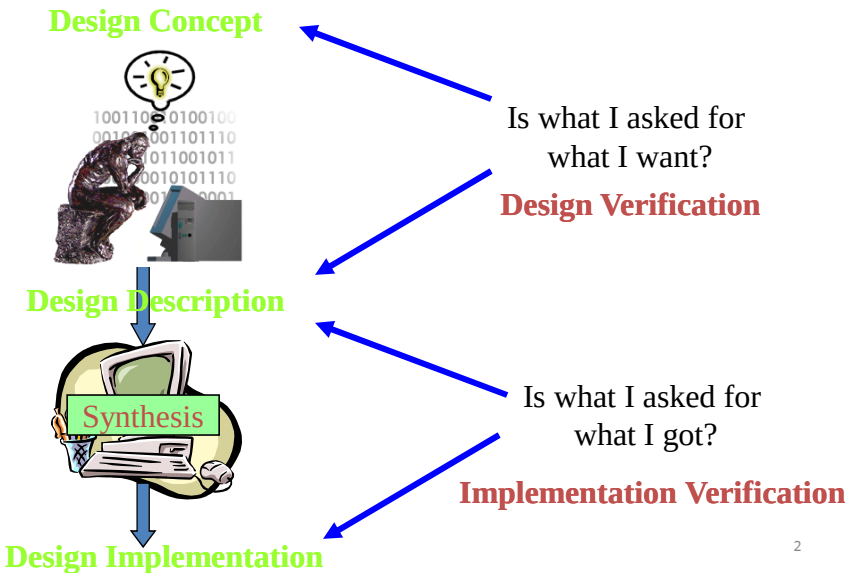
# Digital Systems Verification

## Major Verification Tasks



# Digital Systems Verification

- Overview
  - Cycle-based and event-driven simulation
  - Formal methods
- Timing Analysis
- Hardware Description Languages (Verilog-VHDL)
- System C

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## Digital Systems Verification
## Timing Analysis

- Not only has the design to "function properly"….it also has always tighter timing constraints

- Design timing properties have to be verified

⇒ Static Timing Analysis is the main method

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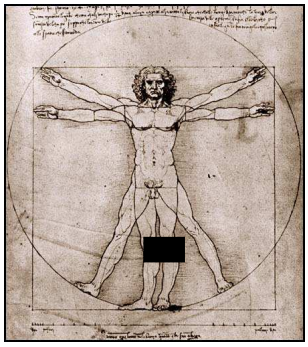
## Physical issues verification (DSM)

- Interconnects
- Signal Integrity
  - P/G integrity
  - Substrate coupling
  - Crosstalk
- Parasitic Extraction
- Reduced Order Modeling
- Manufacturability and Reliability
- Power Estimation



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## Physical issues verification (DSM)
## Interconnects

- Scaling technology
  - They get longer and longer
  - Increasing complexity
  - New materials for low resistivity

  → Inductance and capacitance become more relevant

- Larger and larger impact on the design

  ⇒ Need to model them and include them in the design choices (gate-centric to interconnect-centric paradigm)

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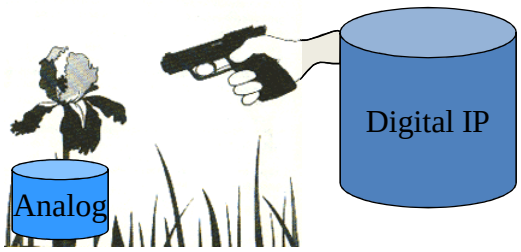
## Physical issues verification (DSM)
### P/G and Substrate

- Analog and Digital blocks may share supply network and substrate
- Can I just plug them together on the same chip? Will it work?
- The switching activity of digital blocks injects noise current that may "kill" analog sensitive blocks

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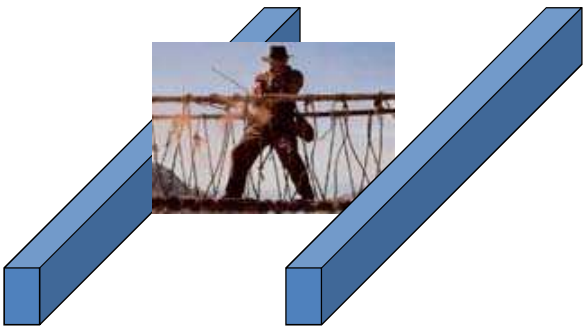
## Physical issues verification (DSM)
### Crosstalk

- In DSM technologies, coupling capacitance dominates interlayer capacitance

  ⇒ there is a "bridge" between interconnects on the same layer….they interfere with each other!



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## Physical issues verification (DSM)
## Parasitic Extraction

- Parasitics play a major role in DSM technologies

- Need to properly extract their value and model

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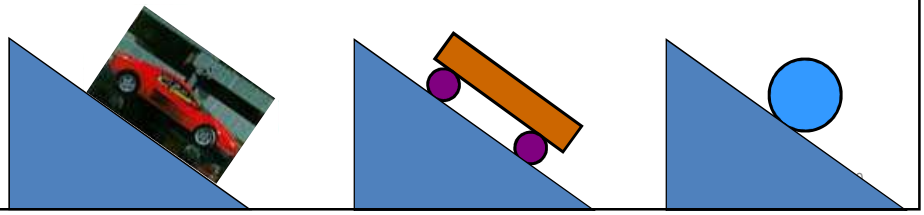
## Physical issues verification (DSM)
## Reduced Order Modeling

- Increasing complexity $\Rightarrow$ bigger and more complex models
  - E.g. supply grid, parasitics…
- Need to find a "reduced" model so that
  - Still good representation
  - Manageable size



## Physical issues verification (DSM)
## Manufacturability

- Design a chip
- Send it to fabrication
- …….
- Did I account for the fabrication process variations?
- How many of my chips will work?
  - Just one? All? Most of them?
- How good is my chips performance?

⇒Design and verification need to account for process variations!

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## Physical issues verification (DSM)
## Reliability

- Design a chip
- Send it to fabrication
- …….
- Did I test my design for different kinds of stress?
- Is it going to work even in the worst case?
- Can I sell it both in Alaska and Louisiana?

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**Physical issues verification (DSM)**

**Power Estimation**

- Advent of portable and high-density circuits
  $\Rightarrow$ power dissipation of VLSI circuits becomes a critical concern

- $\Rightarrow$Accurate and efficient power estimation techniques are required